Title: MEMORY MANAGEMENT FOR SYSTEMS FOR GENERATING 3-DIMENSIONAL COMPUTER IMAGES
Inventor(s): Stephen MORPHET
Serial No.: Unknown
Docket No.: R&G C-327A

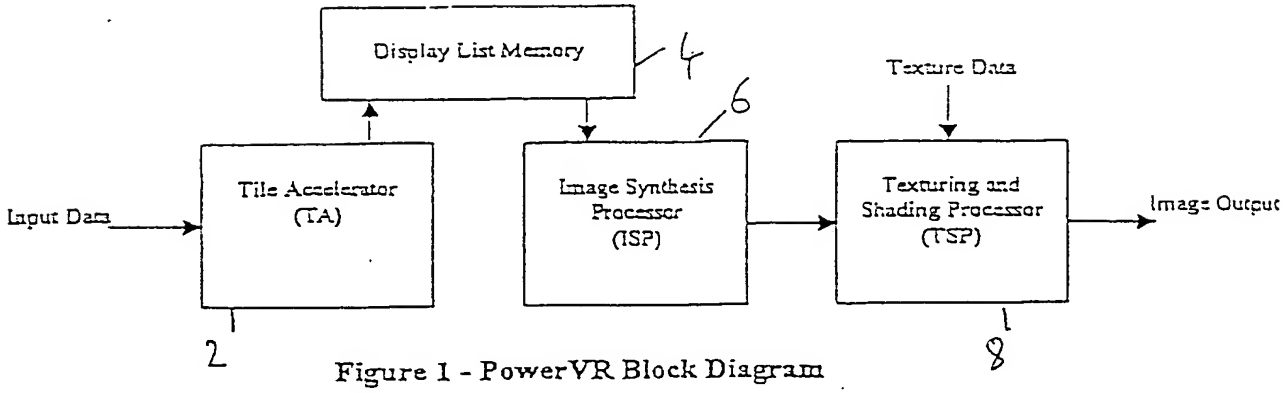


Figure 1 - PowerVR Block Diagram

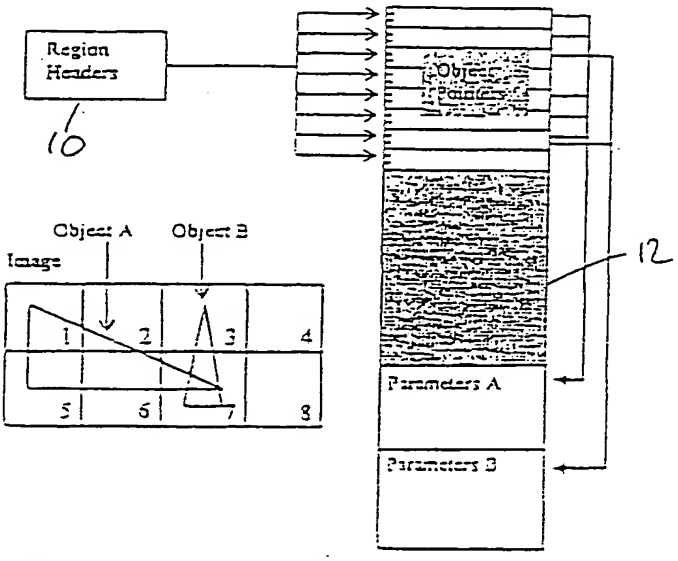


Figure 2 - Conventional PowerVR Tiling

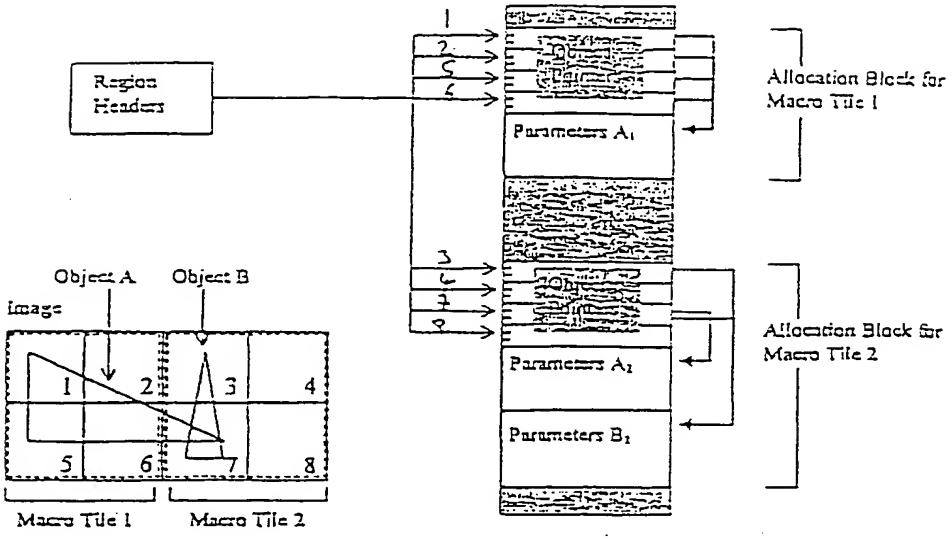


Figure 3 - Macro Tiling

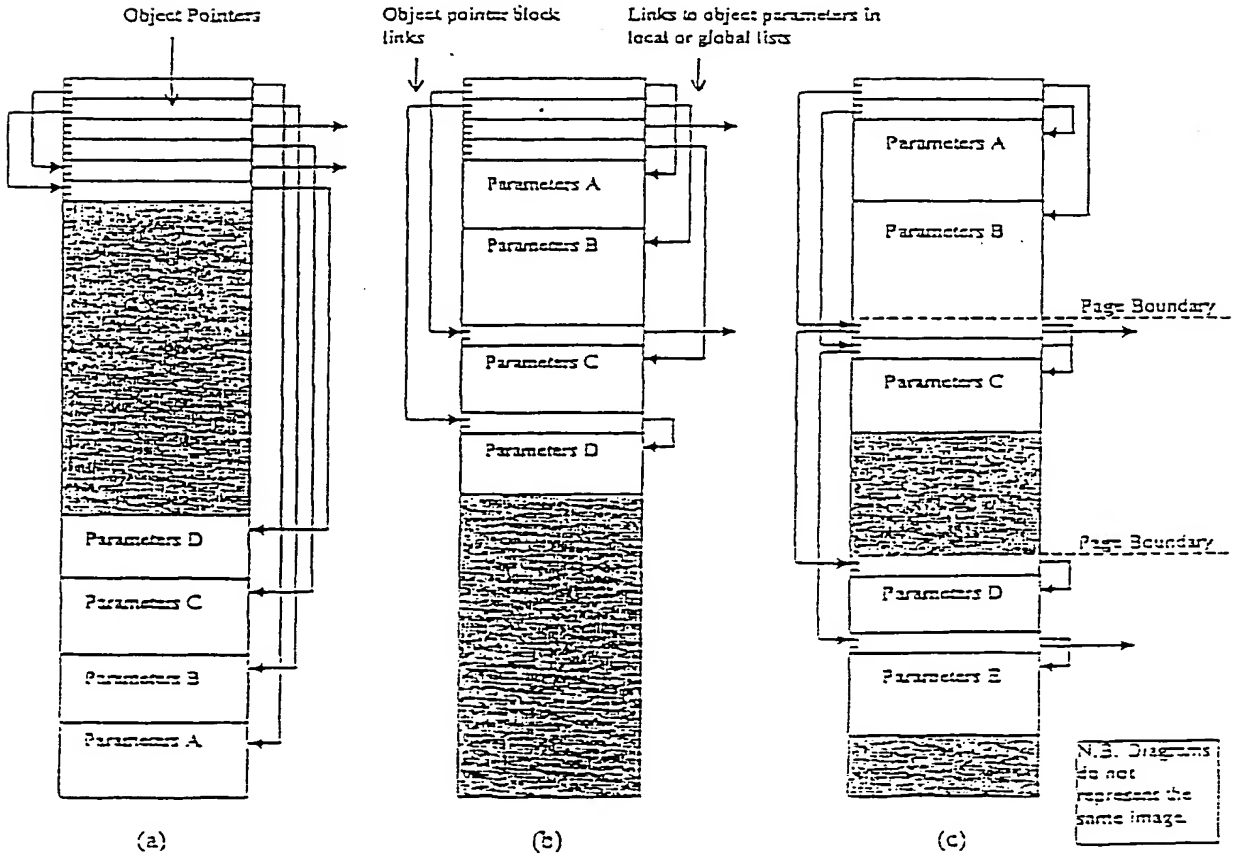


Figure 4 – Alternative Object Pointer Layouts

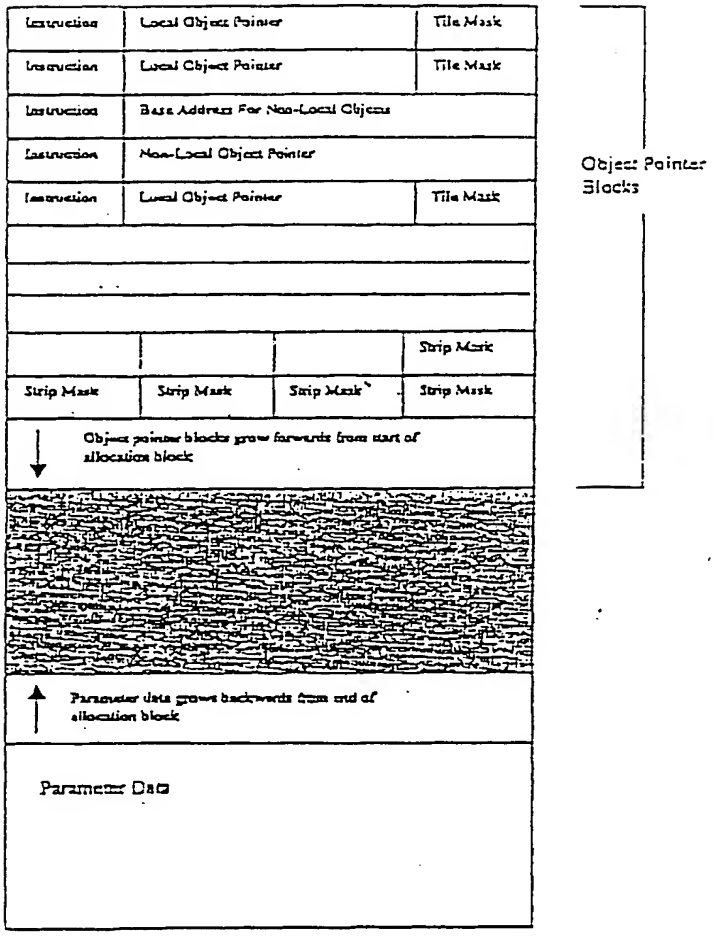
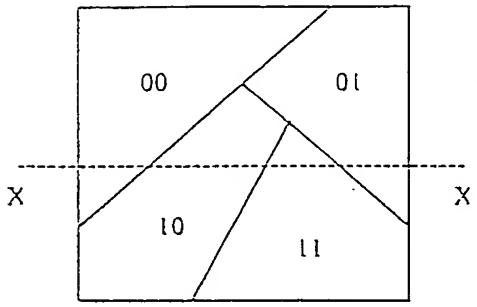


Figure 5 - Object Pointer Storage Using A Single List



Tile with bitmap for four polygons.

Polygon Parameters:

$00 - A_{00}\ B_{00}\ C_{00}$
$01 - A_{01}\ B_{01}\ C_{01}$
$10 - A_{10}\ B_{10}\ C_{10}$
$11 - A_{11}\ B_{11}\ C_{11}$

Depth profile along line XX shown in Figure ~~XIb~~ 7.

Figure ~~X~~6a: Z Compression by storing triangle plane parameters.

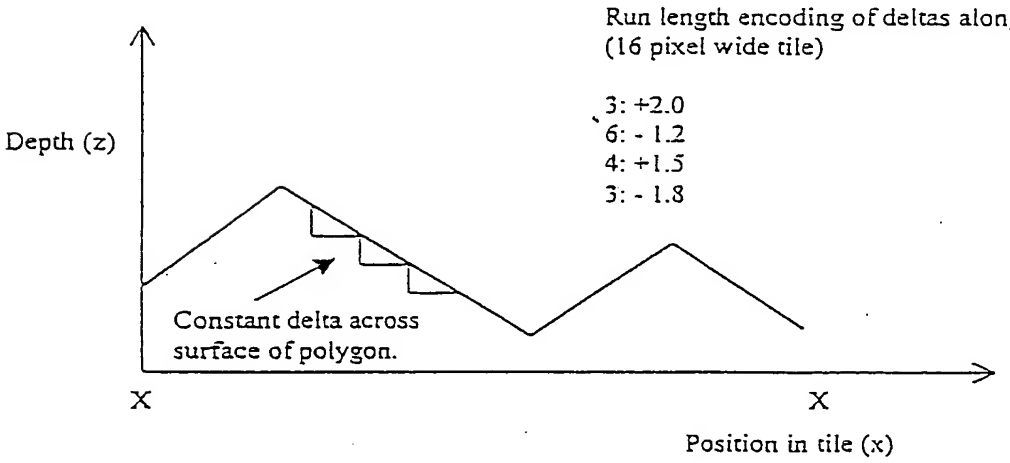


Figure ~~X~~7b: Z compression by run length encoding of delta values. (not to scale).

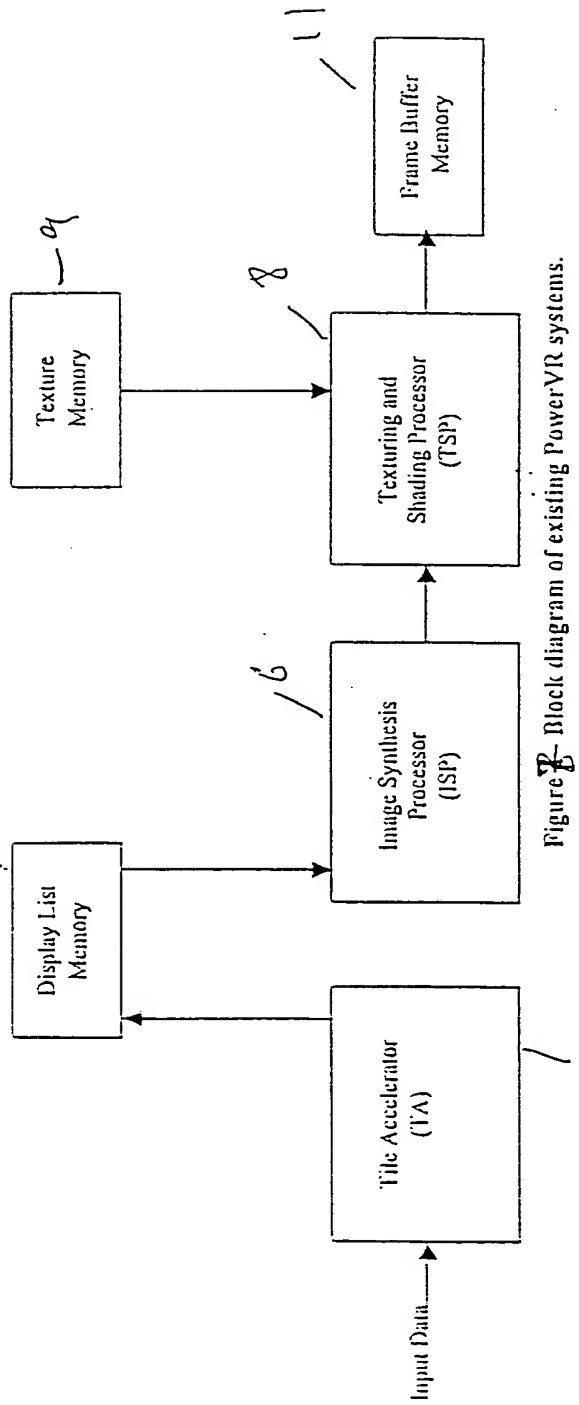


Figure 8 Block diagram of existing PowerVR systems.

Figure 8

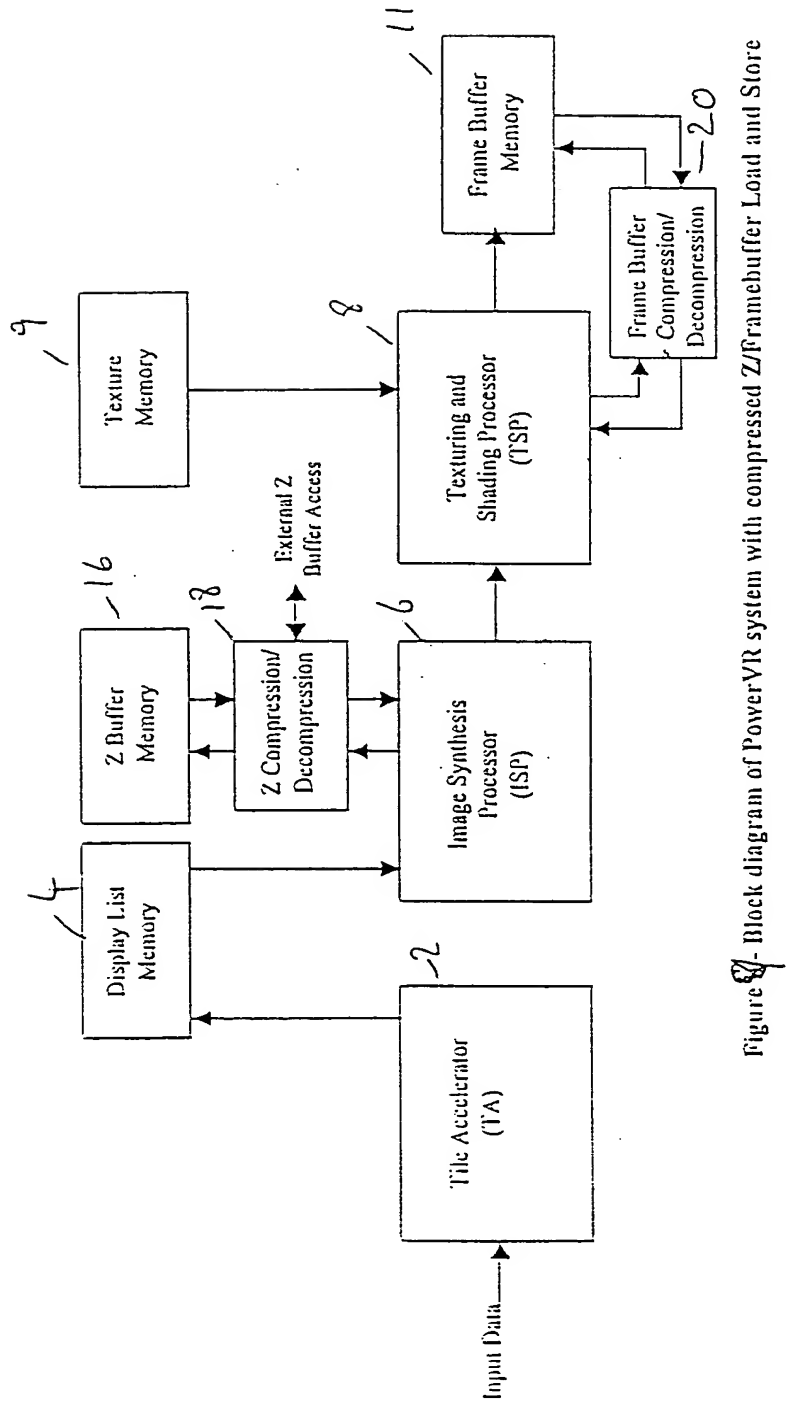


Figure 8 - Block diagram of PowerVR system with compressed Z/Framebuffer Load and Store

Figure 9

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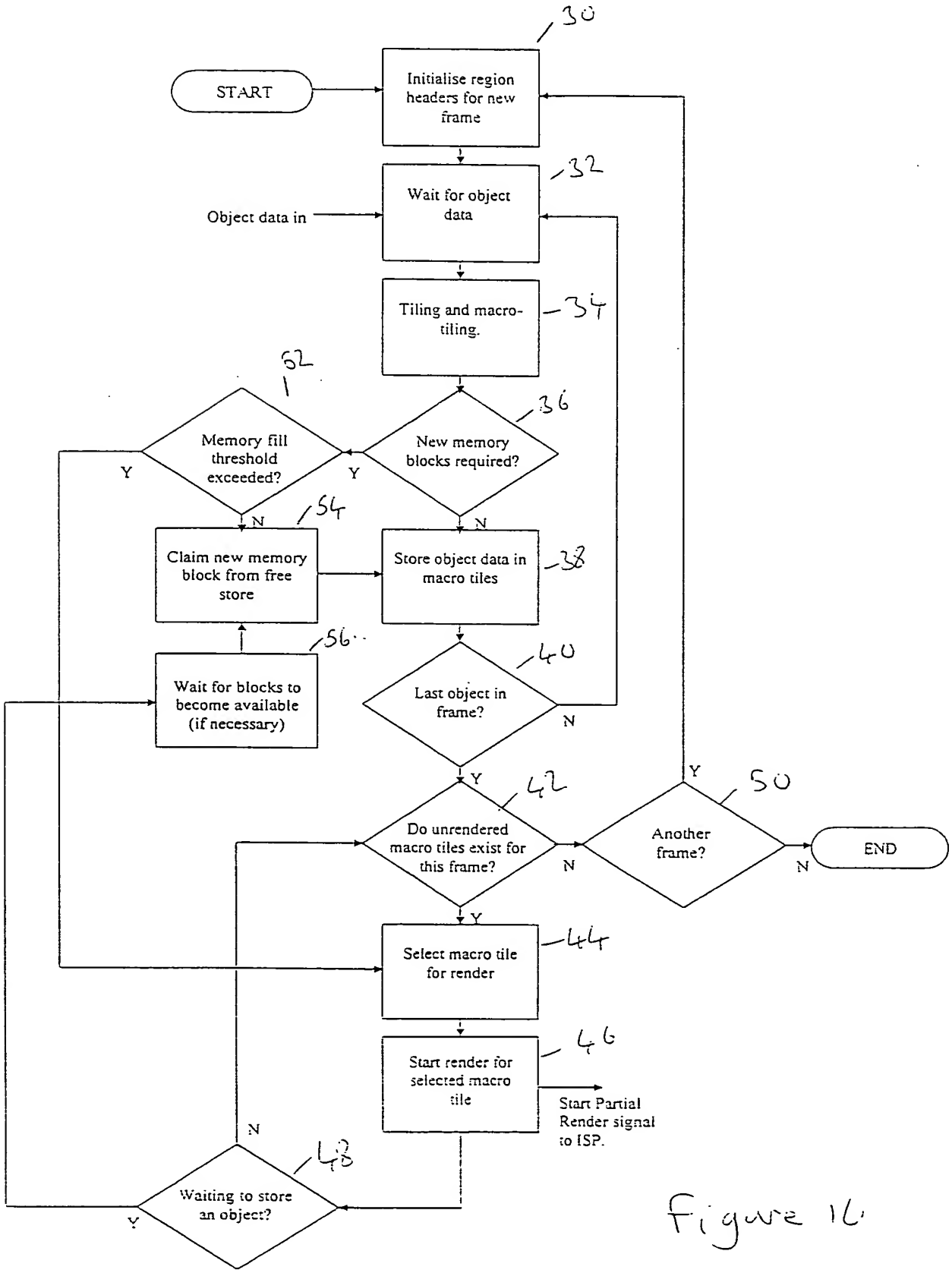

Figure 16

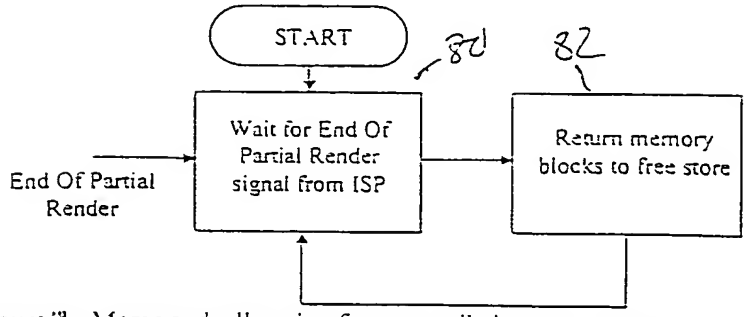

Figure 11 - Memory deallocation for macro tiled memory management.

Figure 11

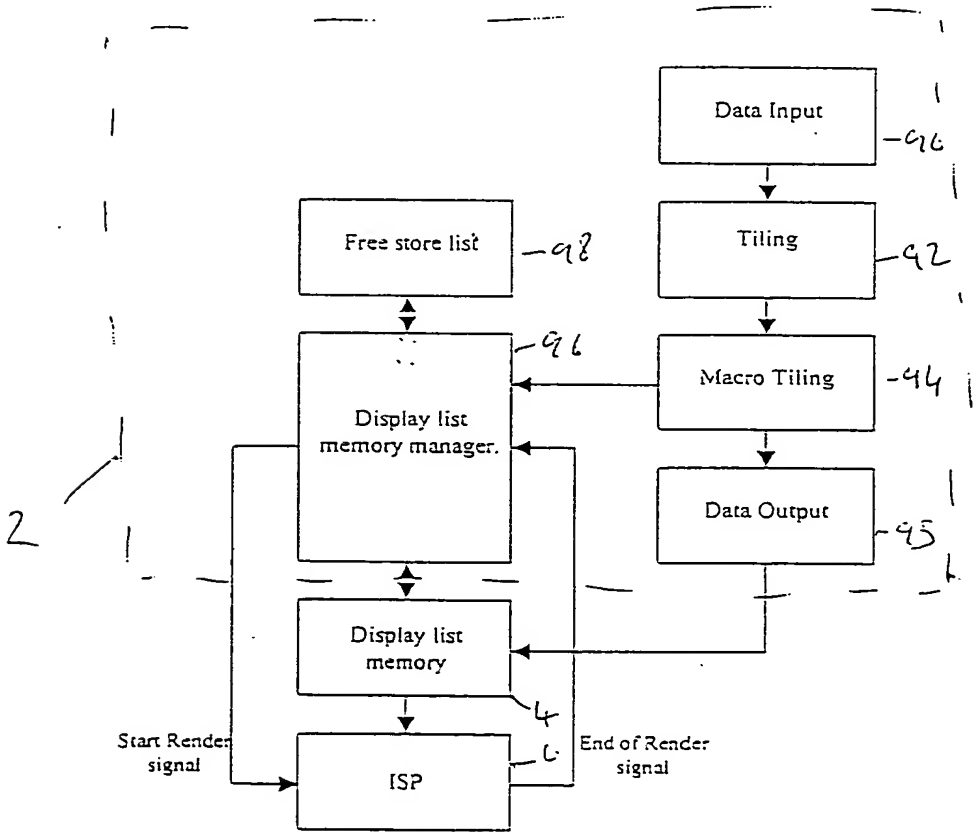

Figure 12 - Block diagram of Tiling Accelerator (TA) with macro tiling

Figure 12